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09/606,367	06/28/2000	Feng Chen	042390.P8530	6023

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EXAMINER
NGUYEN, HIEP

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/606,367	Applicant(s) CHEN ET AL.	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-7 and 10-25* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitations "a plurality of data paths", "a differential circuit", "a differential sense latch", "a differential sense circuit" and " a jam latch" in claim 17, " a differential domino circuit " in claim 19 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 3-6,10-16-20 and 25 are rejected under 35 U.S.C.102 (e) as being anticipated by Takahashi (US Pat. 6037,824).

Regarding claims 1, 3 and 25, figure 7 of Takahashi shows a circuit comprising: a differential sense circuit (231), a latch (233 comprising NAND gates NA2, NA3) said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle. Note that the timing of the storage of data is controlled by clock (icklb0). During operation, the data at the outputs of the sense amplifier portion (231) at nodes (s2, s2b) are held by latch (233) see (col. 12 lines 39-41).

Regarding claim 4, the sense amplifier is a P-type amplifier (N31, P31, N32, P32).

Regarding claim 5, the differential sense circuit comprises a first inverter (P31, N31), the second inverter (P32, N32), the third inverter (IN3) and the fourth inverter (IN4).

Regarding claim 6, the differential sense circuit is symmetrical, thus the loads, in operation, are substantially equivalent.

Regarding claim 10, figure 7 shows a circuit comprising differential circuit comprising a differential domino circuit (P21, N21, P22, N22), the differential domino circuit and the differential sense latch (IN1, IN3, IN4, N33-N35) being coupled such that, in operation, differential output signals present on differential output terminals of the differential domino circuit cause a corresponding electronic signal to be stored in the differential sense latch.

Regarding claims 11 and 12, figure 7 of Katahashi (6,037,824) shows a method for storing electronic signals produced by a differential circuit comprising: pre-charging said differential circuit (elements N12, N13); evaluating said differential circuit (231); sensing differential output signals via a differential sense circuit (231), wherein said differential sense circuit is coupled to a latch (NA2, NA3) in a push-pull configuration (via 231); and storing an electronic signal corresponding to said differential output signal. Transistors (N34, N35) when activated will pull the output approximately the same voltage (ground level).

Regarding claim 13-16, figure 7 of Takahashi (824) shows a method for storing electronic signals produced by a differential circuit comprising: applying clock (iclkb0) after pre-charging to bring the differential output terminal (the drain of N31 to a power supply voltage Vdd) and applying clock (iclkb3) to bring the differential output terminal (the source of N32 to a ground voltage).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by the admitted prior art, figures 1.

Regarding claims 1, 3 and 4, figure 1 of the present application shows a circuit comprising: a differential sense circuit (110), a latch (120, 130) said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle (clock pclk). Amplifier (110) is a p-type amplifier.

Regarding claim 7, figure 1 shows that the amplifier (160) is a n-type amplifier.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 17, 18 and 20-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohshima et al. (US Pat. 6,163,501).

Regarding claims 17, 18 and 20, figures 2, 3 and 6 of Ohshima show an integrated circuit comprising:

a plurality of data paths, (MDQE, bMDQE, MDQO, bMDQ), at least one of said data paths comprising: a differential circuit (21, 22, 23) and

a differential sense latch (24, 25) wherein, the differential sense latch comprises a differential sense circuit (24), a sense amplifier, and a jam-latch latch (25). The jam latch comprises a cross-coupled inverters.

Regarding claim 21-24, the limitations "a processor", "a microprocessor", "a network processor and "a digital processor" are merely intended uses. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparartus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQF.2d 1647 (1987). Therefore, this limitation has not been given patentable weight.

Claim 17, 18 and 20-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al. (US Pat. 6,239,624).

Regarding claims 17, 18 and 20, figure 1of Yang shows an integrated circuit comprising:

a plurality of data paths (inherent in memory circuit), at least one of said data paths comprising: a differential circuit (P1-P4, N1-N3), a sense amp, and

a differential sense latch wherein, the differential sense latch comprises a differential sense circuit (N6-N8) and a jam-latch latch (P5-P8).

Regarding claim 21-24, the limitations "a processor", "a microprocessor", "a network processor and "a digital processor" are merely intended uses. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparartus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQF.2d 1647 (1987). Therefore, this limitation has not been given patentable weight.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (US Pat. 6,037,824).

Regarding claim 7, figure 7 of Takahashi (824) includes all the limitations of the present invention except for the limitation that the sense amplifier comprises an n-type sense amplifier. Figure 7 shows a p-type sense amplifier (P11-P13, N11- N13). However, it is well known the art that the n-type or the p-type sense amplifiers are exchangeable and are used depending on the type of supply voltages and the polarities of input signals. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the n-type sense amplifier to conform to the "high level" control input signals.

Response to Arguments

In the Remarks, the applicant argues that Takahashi (824) "does not recite all of the elements of claim 1 as amended". Claim 1 recites a circuit **comprising** a differential sense circuit and a latch coupled to the differential circuit. Figure 7 of Takahashi fully recites all the elements of claim 1. For instance, a differential sense circuit comprising a sense amplifier portion (231), a latch consisting cross-coupled NAND gates wherein, the latch is coupled to the differential sense circuit (231) to form a differential sense latch. Because the structures of the reference and the claim circuit are similar, the two circuits will perform the same function. Note that in claim 1, the Applicant fails to recite additional components of the "a circuit" that provide performance advantages over the prior art. Claim 11 is not patently distinguished from the reference (figure 7). The precharging is performed by circuit (211). The evaluating is performed by circuit (220. circuit (231) senses differential output signals in a push-pull configuration and the electronic signal is stored in latch (NA2, NA3).

In page 6, the Applicant argues that the N-type, P-type transistors are not exchangeable. According to figures 4 and 5 of the present application, the N-type amplifier (460) and the P-type amplifier (510) are the same except for the polarities of the applied input clocks. Therefore, to accommodate with the polarities of the clock inputs, the proper type of amplifier will be selected. Using N-type or P-type component is seen to be routine design expedient depending on the environment where the circuit is used.

In page 7, first paragraph, the Applicant argues that Takahashi (824) does not disclose a differential sense latch. In fact, figure 7 of Takahashi shows a differential sense latch including a differential sense circuit (231) that senses the differential inputs (node S2 and S2b) and a latch (233).

Allowable Subject Matter

Claims 8-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-9 are objected to because the prior art of record fails to teach or fairly suggest a differential sense amplifier comprising a first and second inverters having stacked n-devices as called for in claim 8.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
12-21-02

TUAN T. LAM
PRIMARY EXAMINER